Reg No:
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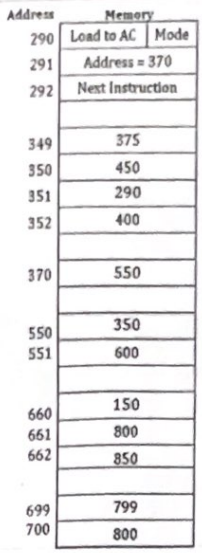
Continuous Assessment Test II – October 2022

Programme	:	**B.Tech. (Computer Science and Engineering)**	Semester	:	**Fall 2022-23**
Course Title	:	**Computer Architecture and Organization**	Course Code	:	**BCSE205L**
			Class Nbr(s)		CH2022231001226/ CH2022231001229/ CH2022231001232/ CH2022231001235/ CH2022231001239/ CH2022231002101
Faculty	:	**Dr. Prabhakar Rao/Prof. Nivedita/Dr. Punitha/ Dr. Monica /Dr Bhavadharini /Dr. Manas**	Slot(s)	:	**C1+TC1**
Time	:	**90 Minutes**	Max. Marks	:	**50**

ANSWER ALL QUESTIONS

1.	Your friend has made a fixed deposit of an amount (P in Rs) in a bank for some period of time (T in years). It is known to your friend that the bank gives a rate of interest (R%) on fixed deposits to each of their customers. Help him calculate the final amount that would be paid to him on the maturity of the fixed deposit. Use the following formula to calculate the maturity amount: $$Maturity\ Amount = P + \frac{P \times R \times T}{100}$$ Device an assembly code using 0-address, 1-address and 2-address instruction format that does this task assuming all the values are stored in the registers. Explain each instruction clearly to achieve the final result. **[4+3+3=10 marks]**	**10**
2.	Figure 1 depicts the memory scenario with addresses in decimal. In this scenario, the program counter value is 290, the R1 register contains 700 and the index register contains 180, find out the effective address of the operand and the operand value with proper justifications by considering the following addressing modes individually. i. Register Indirect addressing ii. Direct addressing iii. Relative addressing iv. Index addressing v. Auto decrement addressing	**10**

	 Fig.1 : Memory Scenario	
3.	Illustrate the architectural design of the Single Cycle Data Path to fetch and execute the following instructions. **MOV AX, R1** **SUB AX, R2** **MOV (R3), AX** Write down the micro routine control sequence steps involved in the architecture with respect to the given instructions. **[4+6=10 marks]**	**10**
4	A *k*-way set associative cache containing 256 blocks uses six bits to represent an offset and seven bits to represent a tag. The main memory address uses 13bits to represent a block number. Assuming each word is byte addressable, compute the following: a) Number of blocks in the main memory **[2 marks]** b) Number of words in each cache block **[2 marks]** c) Size of the cache memory **[2 marks]** d) Size of the main memory **[2 marks]** e) *k*-value for the given scenario **[2 marks]**	**10**
5	i) A company named *Stem* has manufactured a two-level hierarchical cache system (L1 and L2) where the access time of 2 and 10 clock cycles for L1-cache and L2-cache respectively. The miss rate of the L2-cache is one third of the L1-cache with a miss penalty of 50 clock cycles from L2 to main memory. You being the chief designer of the processor, find the miss rate of L1 and L2 if the average memory access time for this cache architecture is 4 clock cycles. **[7 marks]** ii) Is there a need to include multi-level cache in a computer architecture? Justify your answer with the help of a diagram. **[3 marks]**	**10**