Reg. No. [redacted]

Name [redacted]

VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test II – October 2022

Programme	:	**B.Tech. (CSE)**	Semester	:	**Fall 2022-23**
Course Code	:	**BCSE 205L**	Class Number	:	CH2022231001242 CH2022231001243 CH2022231001246 CH2022231001249 CH2022231001252 CH2022231001253
Course Title	:	**Computer Architecture and Organization**	Slot	:	**C2+TC2**
Faculty	:	**Prof. Nivedita/ Dr. Manas/ Dr Bhavadharini/ Dr. Monica/ Dr. Punitha/ Dr. Prabhakar Rao**			
Time	:	**1½ Hours**	Max. Marks	:	**50**

Answer ALL Questions

Q. No.	Question Text	Marks
1.	You have been selected as an assembly language programmer at IM technologies. Your manager has given you an expression: A = (K * Q + R) ÷ (T - H) asking you to code it in one, two and three address instructions. Write the assembly language programs to execute the given expression using the mentioned instruction formats individually and store the result in memory.	**10**
2.	a. Consider two processors (P1 and P2) executing a particular algorithm. The instructions can be divided into four classes along with their frequencies and Cycles Per Instruction given in the table below. P1 has a clock rate of 3 GHz and P2 with a clock rate of 2.5 GHz. Illustrate which implementation is faster? [6 marks] Frequency / CPI of P1 / CPI of P2 Load 20 1 1 Store 30 2 3 Move 30 2 2 Jump 20 1 3 b. A machine has 24 bits instruction format. It has 32 registers and each of which is 32 bit long. It needs to support 49 instructions. Each instruction has two register operands and one immediate operand. Sketch the Instruction format for the above data.[4 marks]	**10**
3.	Consider the memory details given below : **Address** / **Value** 1000 2000 1100 2500 1200 2600 2000 3000 2100 3500 2300 4000 2800 4200	**10**

	Identify the addressing modes for the below mentioned mnemonics i) MOV R1, 3000 ii) MOV R1, [2000] iii) MOV R1, [R2] iv) MOV R1, -200[R2] v) MOV R1, 100[PC] Assume that the initial values of the register R1= 2000, R2=3000, PC=1000.	
4.	A direct mapped cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory has 128K blocks. Compute the bits are there in the tag, block and word fields of the address format. Also find the size of the cache memory (in KB).	**10**
5.	Consider a 4-way set associative cache with a total of 12 cache blocks. The main memory block requests are as follows: 10, 55, 11, 4, 13, 8, 132, 129, 212, 129, 64, 8, 48, 32, 73, 92 Calculate the number of misses and the miss ratio if the replacement strategy is i. Least Recently Used (LRU) [5 marks] ii. First In First Out(FIFO)[5 marks]	**10**

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